CLAIMS

What is claimed is:

1. A method for programming a plurality of non-volatile memory cells in an integrated circuit, the method comprising:

providing a circuit comprising a power pin, a data pin, a ground pin, wherein the plurality of non-volatile memory cells receive binary data provided through the data pin;

applying and maintaining a nominal voltage at the power pin to power the circuit

applying a ground voltage to the ground pin; and

initiating a programming mode to enable the programming by applying a high voltage pulse at the power pin, and applying a high voltage pulse at the data pin while applying the high voltage pulse at the power pin, the high voltage pulses being greater than the nominal voltage.

2. The method of claim 1, further comprising:

after the programming mode is initiated, providing binary data through the data pin to at least one of the non-volatile memory cells;

subsequently providing a high voltage pulse through the data pin to the at least one non-volatile memory cell to program the binary data into the at least one memory cell.

3. The method of claim 2, wherein the binary data is provided to a plurality of the non-volatile memory cells, and then the high voltage pulse is provided to the plurality of the non-volatile memory cells, whereby the same binary data is programmed into the plurality of non-volatile memory cells.

4. The method of claim 1, further comprising:

after the programming mode is initiated, selecting only one of the non-volatile memory cells;

providing binary data through the data pin to the selected non-volatile memory cell;

subsequently providing a high voltage pulse through the data pin at least to the selected non-volatile memory cell to program the binary data into the at least one memory cell.

5. The method of claim 4, wherein the only one non-volatile memory cell is selected by applying a high voltage pulse on the power pin.

6. The method of claim 1, further comprising:

after the programming mode is initiated, sequentially selecting each of the plurality of memory cells for programming until all have been selected one at a time, by applying a series of high voltage pulses on the power pin.

7. The method of claim 6, further comprising;

providing binary data to each of the memory cells at least when the respective memory cell is selected;

subsequently providing a high voltage pulse through the data pin at least to the sequentially selected non-volatile memory cell to program the binary data into the memory cell.

8. The method of claim 6,

wherein while each of the non-volatile memory cells is alone selected, the same binary data is provided to all of the non-volatile memory cells, and then the high voltage pulse is provided to all of the non-volatile memory cells, but only the one selected non-volatile memory cell is programmed with the binary data.

9. The method of claim 1, further comprising:

programming a first said non-volatile memory cell with a first binary data;

subsequently selecting the first non-volatile memory cell;

subsequently selecting a next second memory cell and deselecting the first memory cell without having programmed the first memory cell while it was selected.

10. The method of claim 1, wherein the circuit further comprises a latch coupled between the data pin and the non-volatile memory cells, the latch latches the binary data received through the data pin, and the latch provides the binary data to the non-volatile memory cells.

11. The method of claim 10, further comprising:

after the programming mode is initiated, sequentially selecting each of the plurality of memory cells for programming until all have been selected by applying a series of high voltage pulses on the power pin;

providing the binary data from the latch to each said non-volatile memory cell when the non-volatile memory cell is selected;

programming at least some of the selected non-volatile memory cells with the binary data provided from the latch.

12. The method of claim 11, wherein the step of programming at least some of the non-volatile memory cells comprises providing a high voltage pulse through the data pin to the at least some non-volatile memory cells while selected.

13. The method of claim 10, further comprising:

after the programming mode is initiated, simultaneously selecting a plurality of the non-volatile memory cells;

providing the binary data from the latch to the plurality of the non-volatile memory cells; and

simultaneously programming the selected plurality of the non-volatile memory cells with the binary data provided from the latch.

14. The method of claim 13, wherein the step of programming comprises providing a high voltage pulse through the data pin to the selected plurality of the non-volatile memory cells.

15. A method of programming a non-volatile memory in an integrated circuit, wherein the integrated circuit includes a circuit for programming cells of the non-volatile memory, and the circuit includes a power pin, a data pin, and a ground pin, the method comprising:

receiving a nominal voltage at the power pin to power the circuit;

receiving a ground voltage at the ground pin; and

initiating a programming mode to enable the programming upon receiving a high voltage pulse at the power pin and a high voltage pulse at the data pin while the high voltage pulse is present at the power pin, the high voltage pulses being greater than the nominal voltage.

16. The method of claim 15, further comprising:

after the programming mode is initiated, receiving binary data at the data pin;

providing the binary data to at least one of the non-volatile memory cells;

programming the binary data into the at least one non-volatile memory cell in response to a high voltage pulse received through the data pin.

17. The method of claim 15, further comprising:

after the programming mode is initiated, receiving a series of high voltage pulses on the power pin;

using the series of high voltage pulses to sequentially select each of the plurality of memory cells one at a time for programming, until all the memory cells have been selected.

18. The method of claim 17, comprising:

receiving binary data through the data pin at each of the non-volatile memory cells while the respective non-volatile memory cell is selected;

programming the binary data into each said non-volatile memory cell while the respective non-volatile memory cell is selected in response to a high voltage pulse received through the data pin at the selected non-volatile memory cell.

19. The method of claim 15, further comprising:

storing binary data obtained through the data pin;

subsequently providing the stored binary data to at least one of the memory cells; and

programming the stored binary data into the at least one non-volatile memory cell in response to a high voltage pulse received through the data pin after the binary data is stored.

20. A method of programming a non-volatile memory in an integrated circuit, wherein the integrated circuit includes a circuit for programming cells of the non-volatile memory, and the circuit includes a power pin, a data pin, and a ground pin, the method comprising:

receiving a nominal voltage on the power pin to power the circuit;

receiving a ground voltage on the ground pin;

receiving a series of high voltage pulses on the power pin while the circuit is powered;

using the series of high voltage pulses to sequentially select each of the plurality of memory cells for programming, one said memory cell at a time until all have been selected;

receiving binary data at the data pin, and providing said binary data to each said non-volatile memory cell when selected; and

programming the binary data into at least some of the selected non-volatile memory cells when selected in response to a high voltage pulse received through the data pin.

21. The method of claim 20, further comprising:

simultaneously selecting all of the non-volatile memory cells;

receiving binary data at the data pin, and providing said binary data to the non-volatile memory cells when selected; and

simultaneously programming the binary data into the selected non-volatile memory cells in response to a high voltage pulse received through the data pin.

22. The method of claim 20, wherein the circuit further comprises a latch coupled between the data pin and the non-volatile memory cells, the latch stores the binary data received through the data pin, and the latch provides the binary data to the non-volatile memory cells.

23. The method of claim 20, further comprising:

storing the binary data received through the data pin;

subsequently providing the stored binary data to the selected memory cell;

wherein the high voltage pulse is received by the data pin after the binary data is stored.

24. A programming circuit, in an integrated circuit, for programming non-volatile memory cells of the integrated circuit, said programming circuit comprising:

a power pin through which a nominal voltage is received to power the programming circuit;

a data pin through which a data input of each of the non-volatile memory cells receives binary data;

a ground pin;

a first voltage detector coupled to the power pin for detecting a high voltage applied to the power pin and generating a first signal in response thereto, and a second voltage detector coupled to the data pin for detecting a high applied at the data pin and generating a second signal in response thereto, said high voltages being greater than the nominal voltage; and

a programming control circuit coupled to the first and second voltage detectors, wherein the programming control circuit outputs a third signal when the first and second signals are

coincidentally received by the programming control circuitry, said third signal enabling programming of the non-volatile memory cells.

25. The programming circuit of claim 24, wherein the programming control circuit comprises a state machine, wherein an output of the state machine causes sequential ones of the non-volatile memory cells to be selected for sequential programming.

26. The programming circuit of claim 25, further comprising a decoder coupled to the output of the state machine, and to a select input of each of the non-volatile memory cells, wherein the decoder selects one of the non-volatile memory cells and deselects the remaining non-volatile memory cells based on the outputs of the state machine.

27. The programming circuit of claim 24, wherein the programming control circuit comprises a state machine, wherein an output of the state machine causes all of the non-volatile memory cells to be simultaneously selected for simultaneous programming.

28. The programming circuit of claim 24, further comprising:

a low voltage switch coupled to the data pin that passes only low level voltages to a data input of the non-volatile memory cells, and a high voltage switch coupled to the data pin that passes only high voltages to a programming voltage input of the non-volatile memory cells.

29. The programming circuit of claim 24, further comprising a latch coupled between the data pin and a data input of each of the non-volatile memory cells, wherein the latch temporarily stores binary data received at the data pin while a high voltage pulse is received at the data pin for programming the non-volatile memory cell.

30. A programming circuit, in an integrated circuit, for programming non-volatile memory cells of the integrated circuit, said programming circuit comprising:

a power pin through which a nominal voltage is received to power the programming circuit, and through which a series of high voltage pulses are received;

a data pin through which a data input of each of the non-volatile memory cells receives binary data, and through which a programming voltage input of each of the non-volatile memory cells receives a high voltage pulse;

a ground pin; and

a state machine that receives a clocking signal derived from the series of high voltage pulses received at the power pin, and with each said clocking signal outputs a signal that causes a sequential one or a plurality of the non-volatile memory cells to be selected for programming.

31. The programming circuit of claim 30, further comprising a latch coupled between the data pin and the data input of each of the non-volatile memory cells, wherein the latch stores binary data received at the data pin, and provides the stored binary data to the data input of each selected non-volatile memory cell when the high voltage pulse subsequently is received through the data pin at the programming voltage input of the non-volatile memory cell.